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Accelerated Reliability Assessment for Power Electronics: Optimizing Traditional Testing Methods for EV Applications

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This paper investigates the consistency between commonly used automotive validation methods and the physical degradation mechanisms of power semiconductor devices in electric vehicles (EVs). Current OEM approaches utilizing Power-Thermal-Cycle-Endurance (PTCE) and High-Temperature-Operation-Endurance (HTOE) protocols require a minimum of 6-month validation cycles, conflicting with increasingly compressed 2-year EV production timelines. Field reliability data identifies power semiconductor devices as the most failure-prone components in power electronic converters, accounting for approximately 31% of failures, with dominant mechanisms including bond wire lift-off, solder fatigue, and metallization degradation—all driven by junction temperature (T_j) cycling.

The analysis reveals a fundamental misalignment between system-level testing and junction-driven failure physics. PTCE applies chamber-controlled temperature ramps (2–4 K/min) producing quasi-uniform thermal stress across the assembly, while the dominant semiconductor failure mechanisms require rapid, localized junction temperature swings (10–100 K/s) generated by electrical self-heating. The Coffin-Manson exponent used in system-level testing for OEMs ($c \approx 2$–$2,5$) was empirically derived for bulk solder fatigue, whereas semiconductor-specific failure mechanisms exhibit exponents of $n \approx 3$–7, nearly a factor of two higher. Similarly, HTOE applies a universal activation energy of $E_A = 0,45$ eV, calibrated for packaging-level degradation, while semiconductor-specific mechanisms such as gate oxide (0,6–1,0 eV) and bias temperature instability in SiC (0,6–1,4 eV) operate at fundamentally different energy barriers. Experimental validation on a 800 V/12 V, 3,5 kW DC-DC converter confirms these findings. During PTCE testing (−40 °C to +80 °C, 700 cycles), 65% of measured junction temperature variations fell below 20 K, with only 5% reaching 30–40 K, confirming that the semiconductor is not the primary element subjected to stress. Lifetime estimation using the CIPS08 model with N = 6,88 demonstrates that under field-representative conditions the predicted lifetime exceeds any practical service requirement, while accelerated power cycling at $\Delta T_j = 100$ K compresses validation to approximately 47 days.

For HTOE (80 °C ambient, 120 cycles of 48 h, totaling 240 days), the 48-hour profile reveals that junction temperature reaches only 125 °C during the nominal power phase (33% of cycle, ~16 h), drops to 89 °C during the 31-hour low-power phase, and stabilizes at 80 °C during the 58-minute standby. Despite 5.760 hours of continuous testing, the stress coefficients and test premises do not specifically target semiconductor degradation. Applying the appropriate $E_A = 0,7$ eV for semiconductors at the measured $T_j \approx 105$ °C would reduce test duration from 5.760 to ~3.345 hours—a 42% reduction—while more accurately representing device-level failure physics. Table 1 compares the identified gaps between both methodologies and their semiconductor-specific counterparts. To address these limitations, this work proposes a multi-leg DoE strategy decoupling system and component testing. For PTCE: Leg A validates macroscopic CTE interactions via passive thermal cycling; Leg B focuses on active power cycling at ΔT_j up to +175 °C. For HTOE: Leg A evaluates the full assembly with $E_A \approx 0,4/0,6$ eV; Leg B targets the profile at $T_j = 150$–175 °C $E_A \approx 0,6/1,4$ eV. This approach maintains reliability accuracy while reducing validation time.

Table 1 Identified gaps between system-level and device-level validation

Parameter	PTCE (System)	Active Power Cycling (Device)	HTOE (System)	HTGB (Device)
Thermal stress source	Chamber ramp (2–4 K/min)	Electrical self-heating (10–100 K/s)	Ambient soak at 80–125 °C	Sustained T_j at 150–175 °C
ΔT / T_j range	Assembly-uniform, $\Delta T_j < 40$ K measured	Localized, ΔT_j = 80–150 K	T_j = 89–125 °C profile dependent	T_{jmax} rated (150–175 °C)
Acceleration model	Coffin-Manson, c = 2–2,5	CIPS08 model, n = 3–7	Arrhenius, E_A = 0,45 eV	Arrhenius, E_A = 0,7–1,4 eV
Failure mechanisms targeted	Bulk solder, housing, seals, connectors	Wire bonds, die attach, metallization	Solder IMC, polymer aging, contact drift	Gate oxide TDDB, BTI, Vth drift
Detection capability	Functional pass/fail	ΔR_DS(on) +5%, ΔR_{th} +20%	Functional pass/fail	ΔV_{th}, $\Delta R_{DS(on)}$, ΔBV_{DSS}
Typical test duration	175 days (700 cycles)	~47 days at ΔT_j = 100 K	240 days (5.760 h)	~40 days (1.000 h)
Semiconductor representativeness	Low — 95% of cycles below 30 K	High — targeted ΔT_j at die level	Low — E_A underestimates by 0,2–0,9 eV	High — mechanism-specific stress