

Considerations and Countermeasures for Reliability Design of BGA Solder Joints.

Hisao Nishimori¹⁾ Jun Muto¹⁾ Yasufumi Shibata¹⁾

*1) Toyota Motor Corporation
1, Toyota-cho, Toyota, Aichi, 471-8572 Japan*

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The increasing adoption of Software Defined Vehicles (SDVs) has accelerated the demand for high-performance processors and large-capacity memory devices in automotive Electronic Control Units (ECUs). To accommodate the growing number of terminals required by these devices, Ball Grid Array (BGA) package integrated circuits are widely employed because of their high-density interconnection capability. However, BGA solder joints are located beneath the package and cannot be visually inspected after assembly, making it difficult to verify solder joint quality during mass production. Because automotive electronic products require long-term reliability under severe operating conditions, it is essential to incorporate solder joint quality into the design and manufacturing process from the early development stage. This study investigates failure modes associated with BGA solder joints through both destructive and non-destructive analyses and discusses reliability-design approaches based on failure-mode understanding and international standards.

Cross sectional analysis of a functionally defective BGA package revealed a very thin lift-off region near the alloy interface between the copper pad on interposer board and the solder ball. To evaluate the occurrence and characteristics of this defect, three different BGA package ICs were analyzed using an ink penetration and pull method. After immersion in dye, drying, and separation from the printed circuit board, fracture surfaces were classified into five fracture modes designated A through E. The observed defect corresponded to Mode B fracture, which occurred in approximately 2 – 7 % of the evaluated solder joints. Detailed observation of the peeled surfaces revealed dye penetration on fracture interfaces where no dye should have been present in a sound solder joint, suggesting the existence of localized interfacial separation prior to fracture. X-ray inspection was subsequently conducted to assess the detectability of the defect by non-destructive means. Although X-ray images successfully identified voids and wiring structures, no obvious indication of the thin interfacial lift-off could be detected, even in samples later confirmed to contain Mode B failures through destructive analysis. These findings indicate that conventional inline X-ray inspection alone may not be sufficient to identify very thin delamination like defects in BGA solder joints. As automotive electronics continue to become more complex, reliability assurance must rely not only on manufacturing inspections but also on a design oriented understanding of potential failure mechanisms. Analysis of occurrence trends showed that larger BGA packages, particularly those with hundreds of solder balls, may exhibit a tendency for failure concentration near peripheral ball locations where warpage-induced stress is generally higher. Consequently, package warpage, local stress concentration, PCB structural design, and via configuration should be considered carefully during reliability design reviews.

Furthermore, systematic utilization of international standards such as IPC-7095 and IPC-TM-650 2.4.53 provides valuable guidance for understanding known failure modes, establishing common evaluation methods, enhancing FMEA and FTA activities, improving engineering education, and preventing oversight of latent reliability risks. The results of this study demonstrate that effective BGA solder joint reliability assurance requires an integrated approach combining failure-mode analysis, reliability oriented design practices, complementary destructive verification methods, and continuous knowledge sharing through international standards activities. Such an approach contributes to more robust automotive electronic products while reducing unnecessary quality problems and supporting the development of future high-reliability ECU designs.

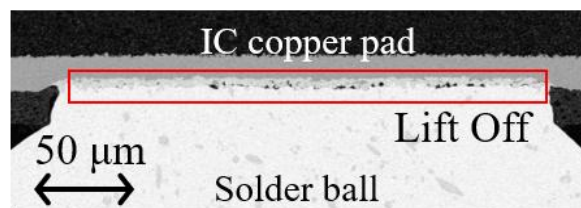


Fig.1 Cross section photo of BGA joint malfunction.

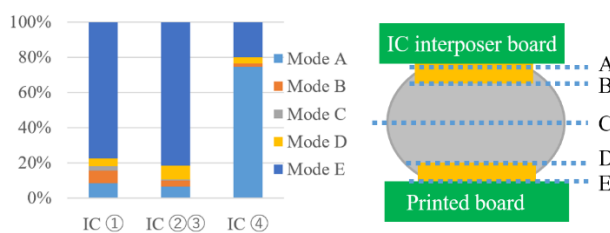


Fig.2 Definition of destruction mode of the peeled analysis (right) and graphs of the destruction mode occurrence rates at each ICs (left).

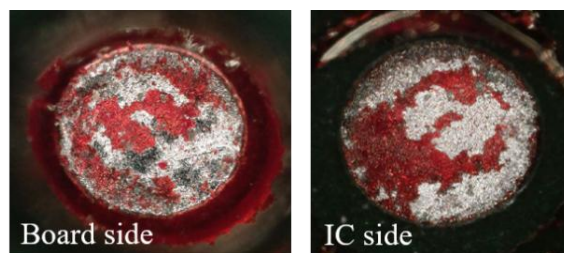


Fig.3 Results of the peeled surface observation which are the board side (left) and the IC side (right).